Amendments to the Claims

1-26. (Canceled)

27. (Currently Amended) A high-availability cellular computer system capable of automatically updating firmware in cells of the system, the system comprising:

a high speed interconnect;

a management interconnect;

a first cell and a second cell, each cell comprising at hardware level:

at least one processor of the cell coupled to at least one random-access memory subsystem of the cell,

at least one nonvolatile memory system coupled to the at least one processor of the cell,

a high-speed interconnect interface coupling the at least one processor of the cell to the high speed interconnect;

a management processor of the cell coupled to a nonvolatile memory for management code of the cell, and

an interface coupling the management processor of the cell to the management interconnect;

wherein the nonvolatile memory ~~subsystem~~ system of the first cell has recorded therein errored firmware ~~selected from the group consisting of outdated or corrupt firmware~~, and the nonvolatile memory ~~subsystem~~ system of the second cell has recorded therein valid firmware; ~~and~~

wherein the first cell contains machine readable code for recognizing that the firmware in the nonvolatile memory system of the first cell is errored firmware and, upon recognizing that the firmware for the first cell is errored, for transmitting over the management interconnect a request for valid firmware to the second cell, and for updating the nonvolatile memory system of the first cell with valid firmware;

wherein the second cell contains machine readable code for recognizing that the firmware in the nonvolatile memory system of the second cell is valid; and

wherein the management code of the second cell comprises machine readable code to

receive a request for valid firmware and, in response thereto, to transmit an acknowledgement via the management interconnect, to enable the high speed interconnect[[;]], and to transmit the firmware in the nonvolatile memory system of the second cell to the first cell via the high speed interconnect.

28. (Previously Presented) The cellular computer system of claim 27 wherein the errored firmware is corrupt firmware.

29. (Previously Presented) The cellular computer system of claim 27 wherein the errored firmware is outdated firmware.

30. (Currently Amended) A high-availability cellular computer system capable of automatically updating firmware in cells of the system, the system comprising:

a physical high speed interconnect;

a physical manageability interconnect;

a first cell and a second cell, each cell comprising at least one physical processor coupled to

at least one physical random-access memory subsystem of the cell,

at least one physical nonvolatile memory system of the cell,

a high-speed interconnect interface, and

a cell manageability subsystem coupled to the manageability interconnect, the cell manageability subsystem comprising a cell manageability processor;

wherein the high-speed interconnect interface of the first cell and the second cell is coupled to the high speed interconnect; ~~and~~

wherein the nonvolatile memory ~~subsystem~~ system of the first cell has recorded therein errored firmware, and the nonvolatile memory ~~subsystem~~ system of the second cell has recorded therein valid firmware; ~~and~~

wherein the first cell contains machine readable code for recognizing that the firmware in the nonvolatile memory system of the first cell is errored and, upon recognizing that the firmware of the first cell is ~~corrupt~~ errored, for updating the nonvolatile

memory system of the first cell with firmware copied from a cell having valid firmware;

wherein the second cell contains machine readable code for recognizing that the firmware in the nonvolatile memory system of the second cell is valid; and

wherein the cell manageability processor of the second cell contains machine readable code to receive an update message via the manageability ~~system~~ interconnect and, in response thereto, to transmit an acknowledgement via the manageability ~~system~~ interconnect, to enable the high speed interconnect[[;]], and to transmit the firmware in the nonvolatile memory system of the second cell to the first cell via the high speed interconnect.

31. (Currently Amended) A high-availability cellular computer system capable of automatically updating firmware in cells of the system, the system comprising:

a physical high speed interconnect;

a physical manageability interconnect;

a first cell and a second cell, each cell comprising at least one physical processor coupled to

at least one physical random-access memory subsystem of the cell,

at least one physical nonvolatile memory system of the cell,

a high-speed interconnect interface, and

a cell manageability subsystem coupled to the manageability interconnect, the cell manageability subsystem comprising a cell manageability processor;

wherein the high-speed interconnect interface of the first cell and the second cell is coupled to the high speed interconnect; ~~and~~

wherein the nonvolatile memory ~~subsystem~~ system of the first cell has recorded therein errored firmware, and the nonvolatile memory ~~subsystem~~ system of the second cell has recorded therein valid firmware; ~~and~~

wherein the first cell contains machine readable code for recognizing that the firmware in the nonvolatile memory system of the first cell is ~~corrupt~~ errored and, upon recognizing that the firmware of the first cell is errored, for updating the

nonvolatile memory system of the first cell with firmware copied from a cell having valid firmware;

wherein the second cell contains machine readable code for recognizing that the firmware in the nonvolatile memory system of the second cell is valid; and

wherein the cell manageability processor of the second cell contains machine readable code to receive an update message via the manageability ~~system~~ interconnect and, in response thereto, for transmitting the firmware in the nonvolatile memory system of the second cell to the first cell via the manageability interconnect.

32. (Currently Amended) A high-availability cellular computer system capable of automatically updating firmware in cells of the system, the system comprising:

a high speed interconnect;

a manageability interconnect;

a first cell and a second cell, each cell comprising at hardware level:

at least one processor of the cell coupled to at least one random-access memory subsystem of the cell,

at least one nonvolatile memory system coupled to the at least one processor of the cell,

a high-speed interconnect interface coupling the at least one processor of the cell to the high speed interconnect, and

a cell manageability processor coupled to the manageability interconnect;

wherein the high-speed interconnect interface of the first cell and the second cell is coupled to the high speed interconnect; ~~and~~

wherein the nonvolatile memory ~~subsystem~~ system of the first cell has recorded therein corrupt firmware, and the nonvolatile memory ~~subsystem~~ system of the second cell has recorded therein valid firmware; ~~and~~

wherein the first cell contains machine readable code for recognizing that the firmware in the nonvolatile memory system of the first cell is corrupt and, upon recognizing that the firmware of the first cell is corrupt, for updating the nonvolatile memory system of the first cell with firmware copied from a cell having valid firmware;

wherein the second cell contains machine readable code for recognizing that the firmware

in the nonvolatile memory system of the second cell is valid; and

wherein the ~~management~~ cell manageability processor of the second cell has machine readable code to receive an update message via the manageability ~~system~~ interconnect and, in response thereto, to transmit an acknowledgement via the manageability ~~system~~ interconnect, to enable the high speed interconnect[[;]], and to transmit the firmware in the nonvolatile memory system of the second cell to the first cell via the high speed interconnect.

33. (Previously Presented) A method for updating firmware in a cellular, high availability, computing system comprising:

providing a plurality of cells of a cellular computing system, where each cell has firmware and comprises:

at least one processor,

a random-access memory coupled to the at least one processor,

a management processor, and

a high-speed interconnect interface;

determining a first cell of the plurality of cells having errored firmware, and an update cell of the plurality of cell having desired firmware;

sending a firmware update request from the management processor of the update cell over a management interconnect to the management processor of the first cell; and

transmitting the desired firmware from the update cell through a high-speed interconnect into the first cell;

wherein the high-speed interconnect is distinct from the management interconnect, and during normal operation of the computing system is used for communications between a plurality of cells of the computing system.

34. (Previously Presented) The method of claim 33 wherein the errored firmware is firmware selected from the group consisting of missing firmware, corrupt firmware, and outdated firmware.

35. (Currently Amended) The method of claim 33 further comprising:

~~when~~ wherein the update cell receives over the management interconnect an acknowledgement of the firmware update request from the first cell prior to transmitting the desired firmware to the first cell.

36. (Previously Presented) The method of claim 35 wherein the step of determining a first cell of the plurality of cells having errored firmware is performed by the management processors of the cells.